ABSTRACT

Methods and apparatuses in which two or more memories share a processor for Built In Self Test algorithms and features are described. The processor initiates a Built In Self Test for the memories. Each memory has an intelligence wrapper bounding that memory. Each intelligence wrapper contains control logic to decode a command from the processor. Each intelligence wrapper contains logic to execute a set of test vectors on a bounded memory. The processor sends a command based self-test to each intelligence wrapper at a first clock speed and the control logic executes the operations associated with that command at a second clock speed asynchronous with the first speed. The processor loads the command containing representations of a march element and data to one or more of the intelligence wrappers via a serial bus.